

Figure 1.: Traditional on-board power distribution.

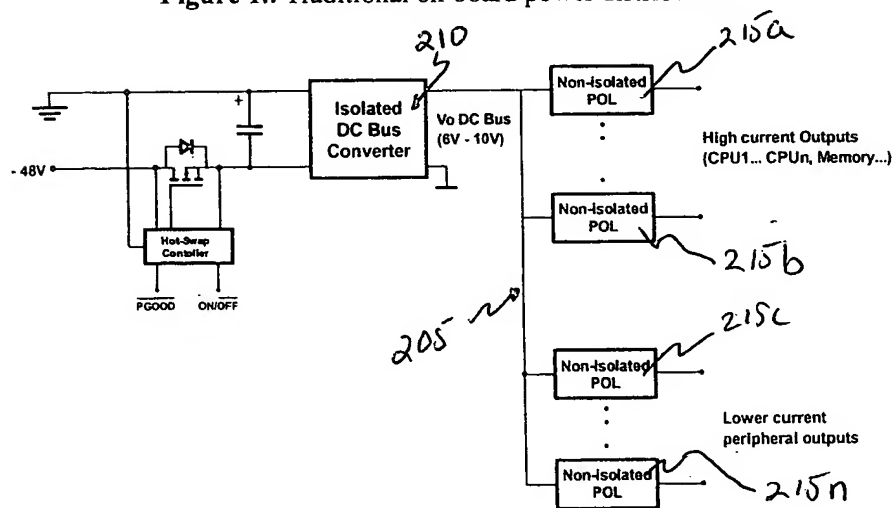


Figure 2

# Optimal distributed power architecture (DPA)

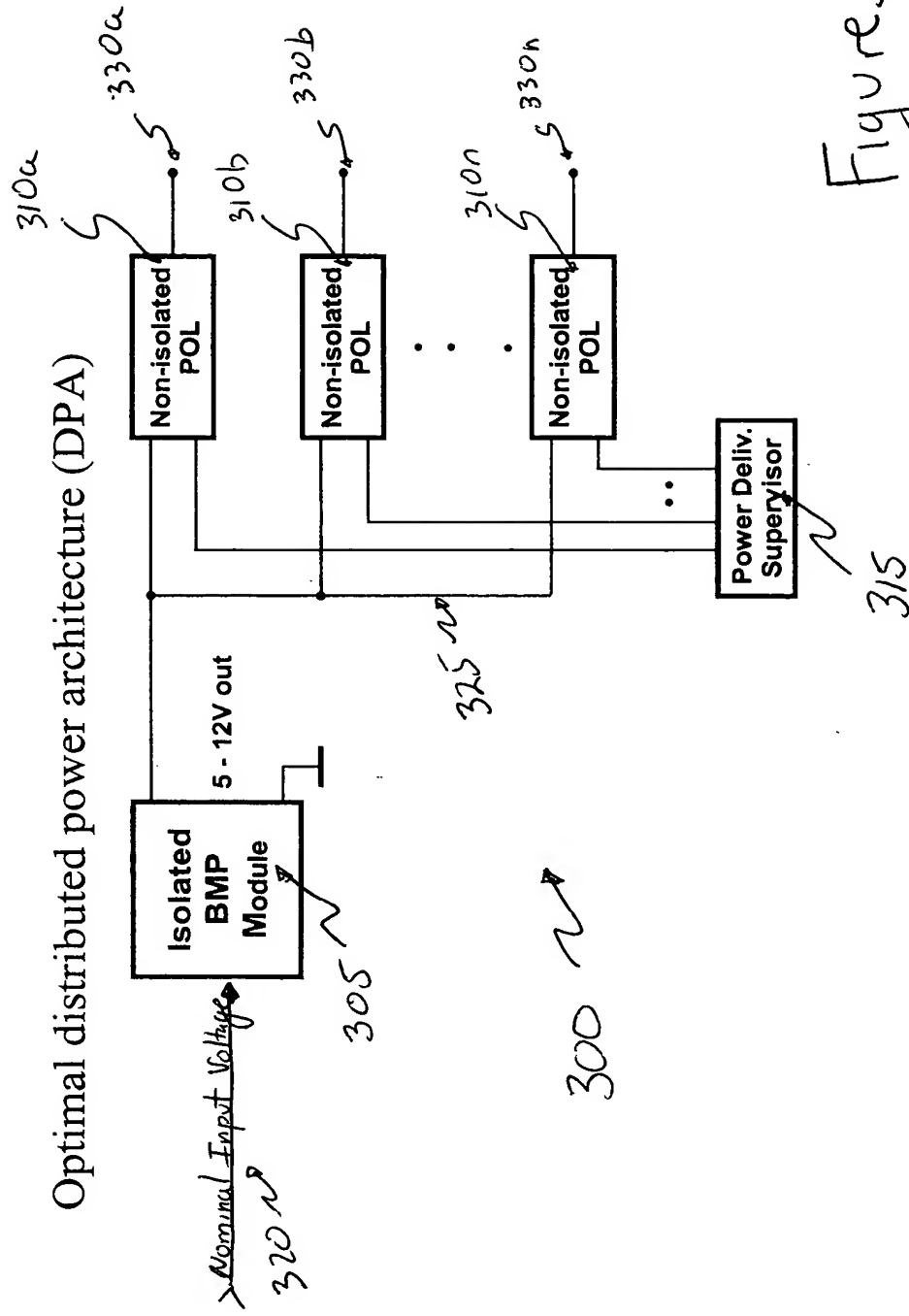


Figure 3

Figure 4

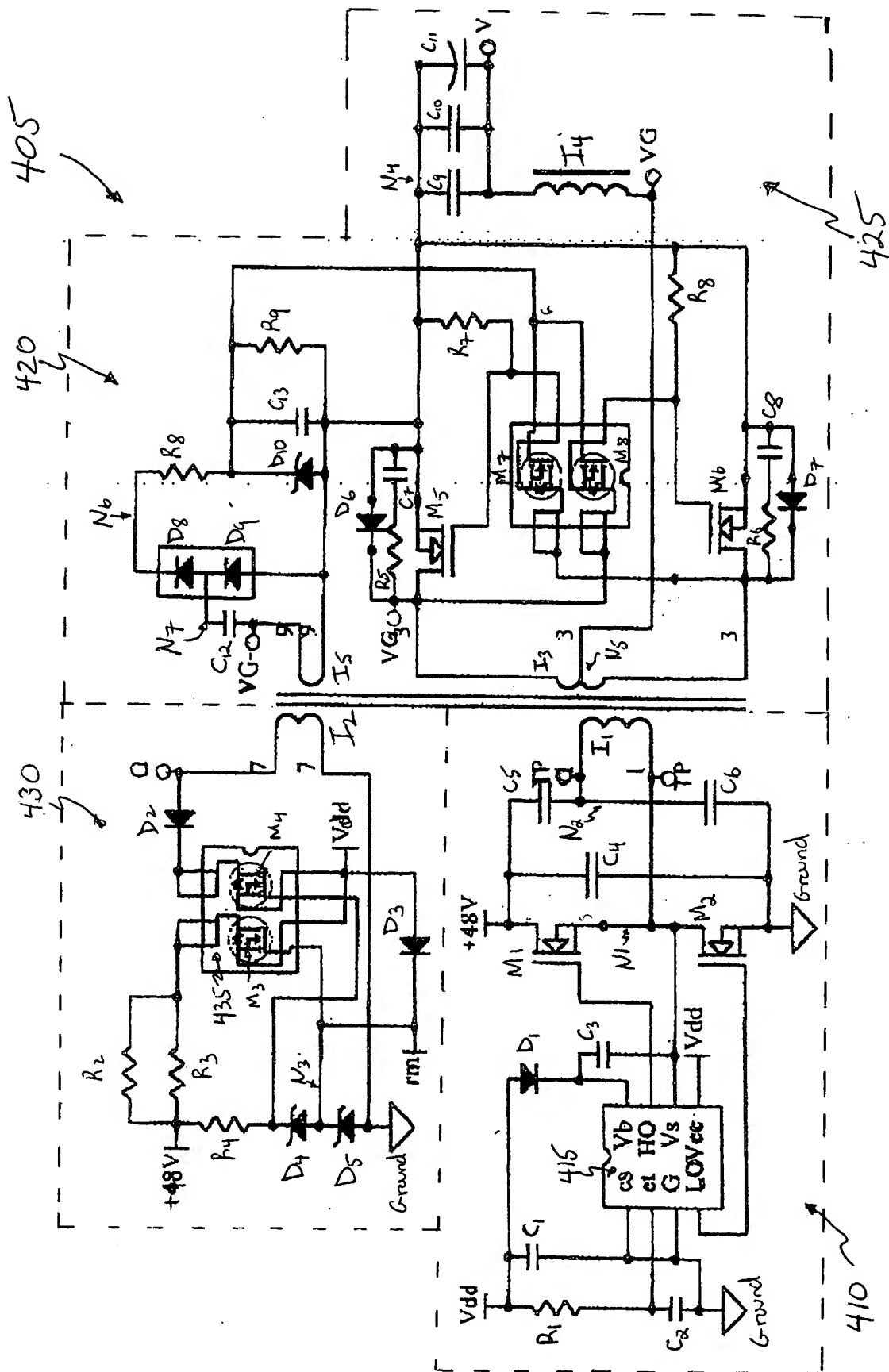


Figure 5

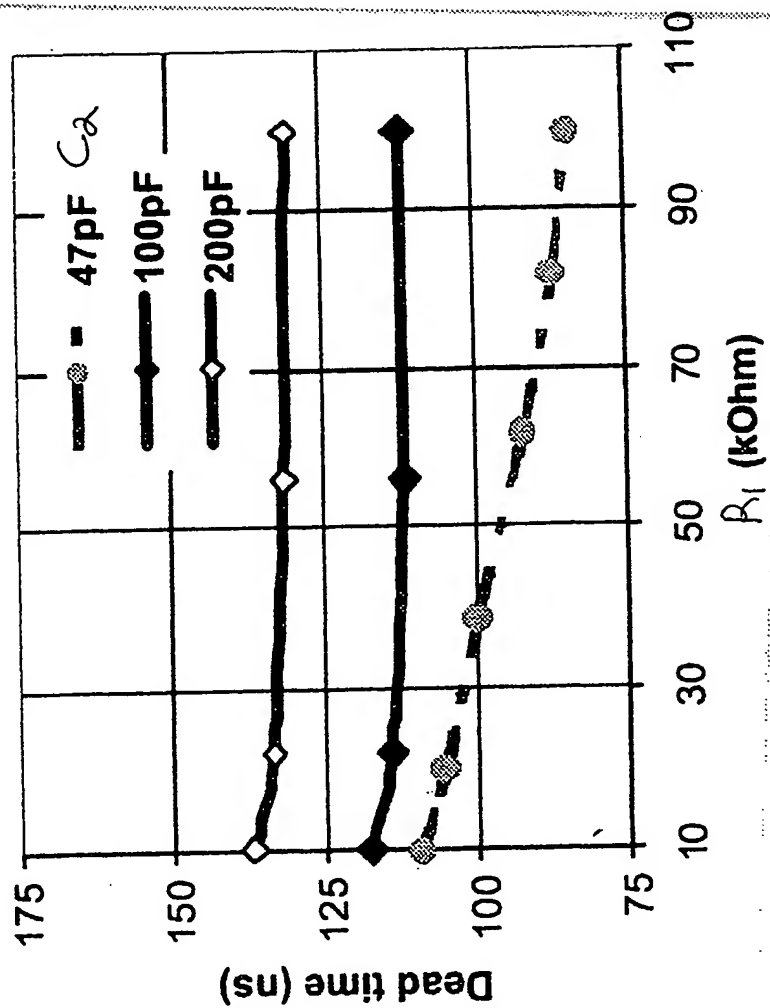
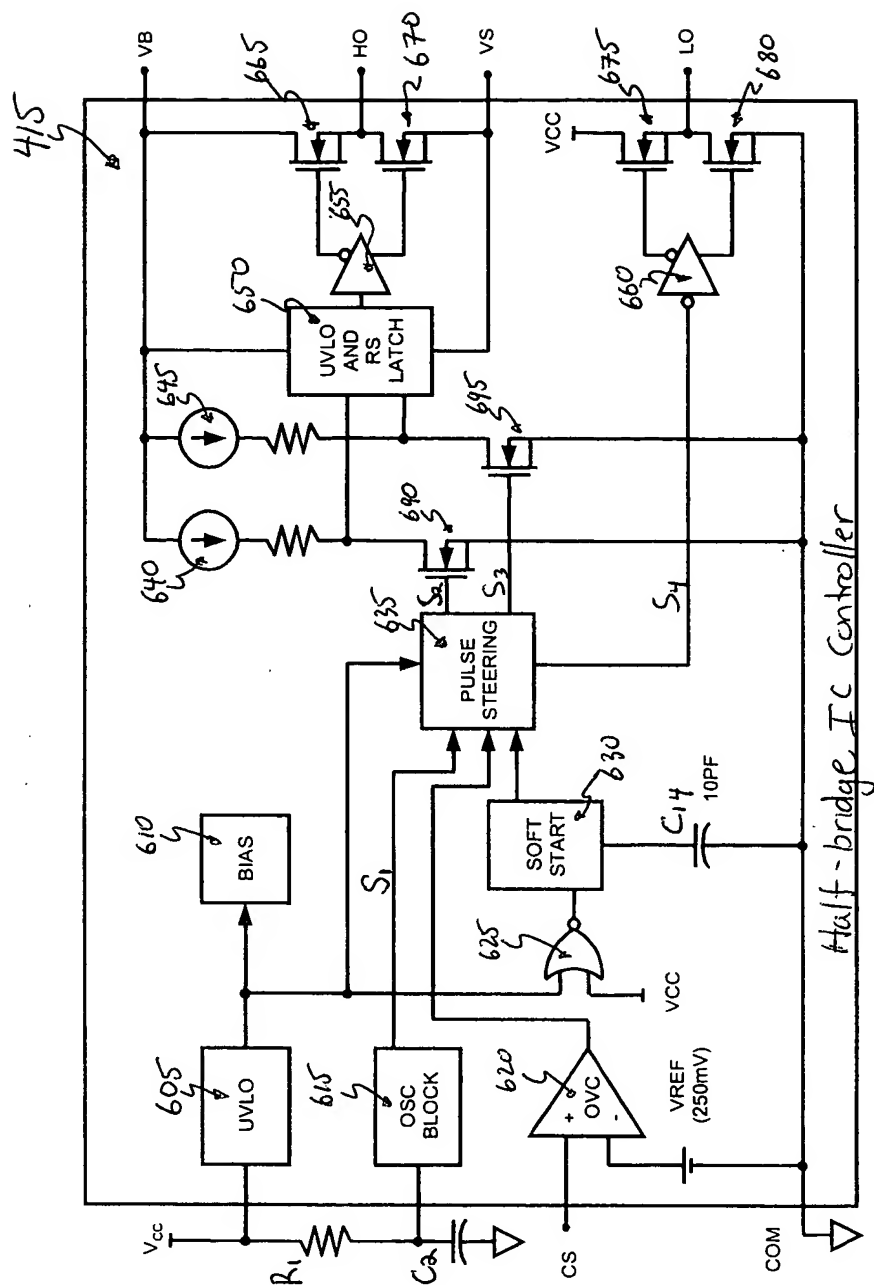


Figure 6



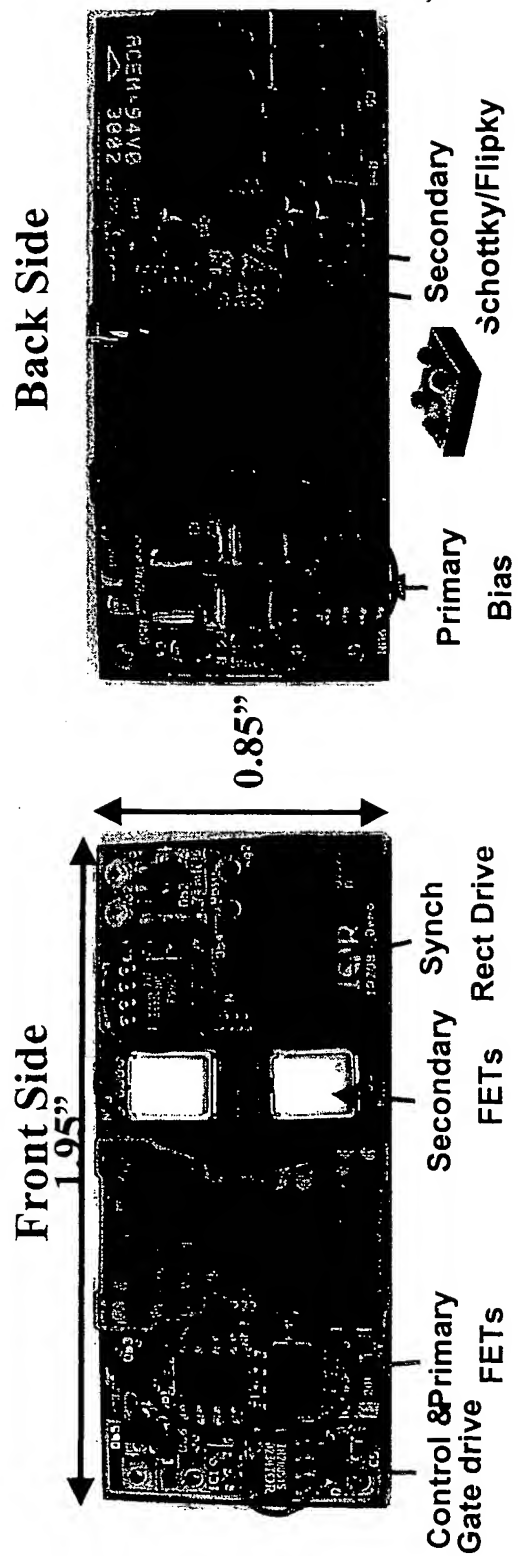
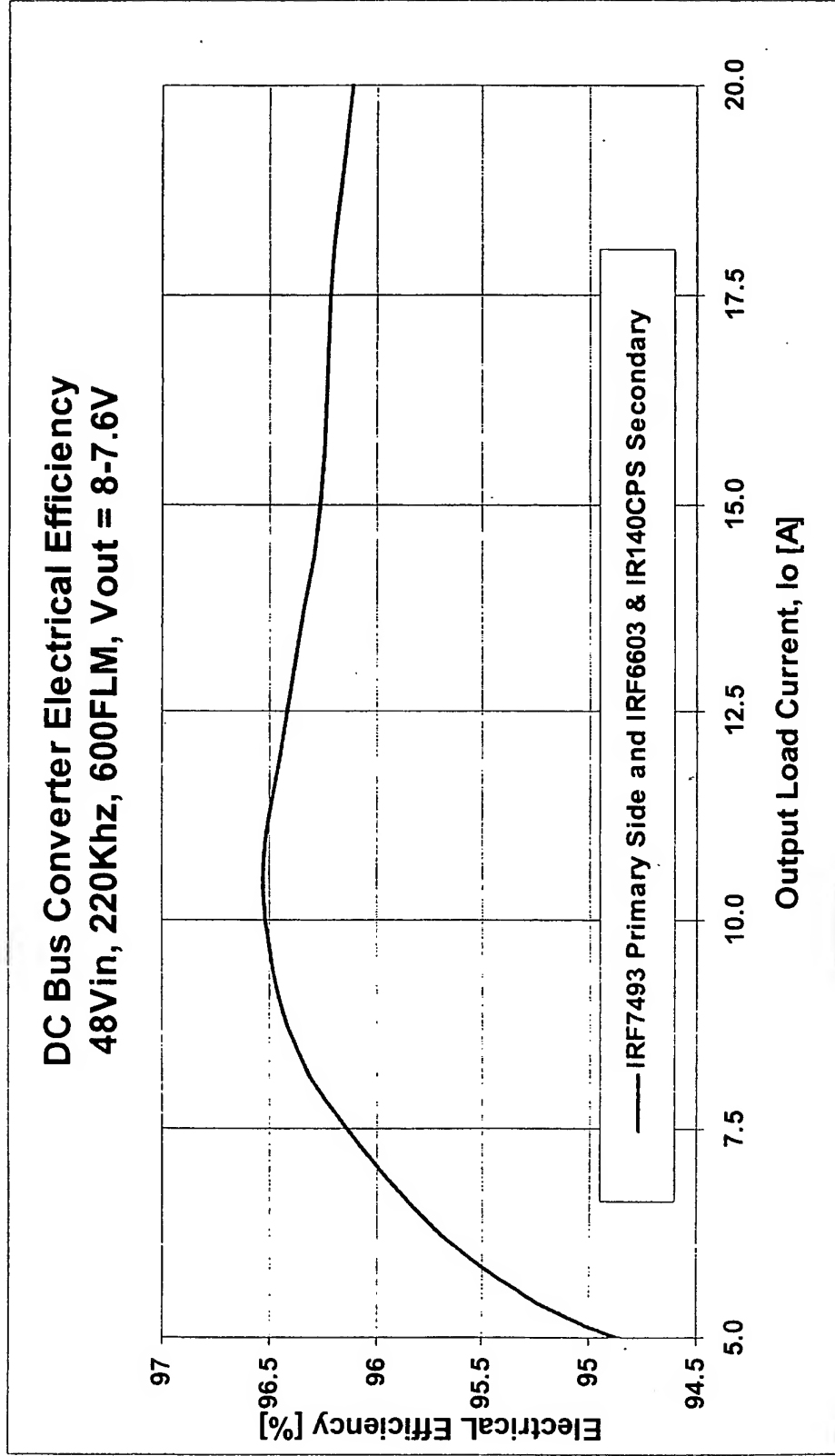


Figure 7

Figure 8



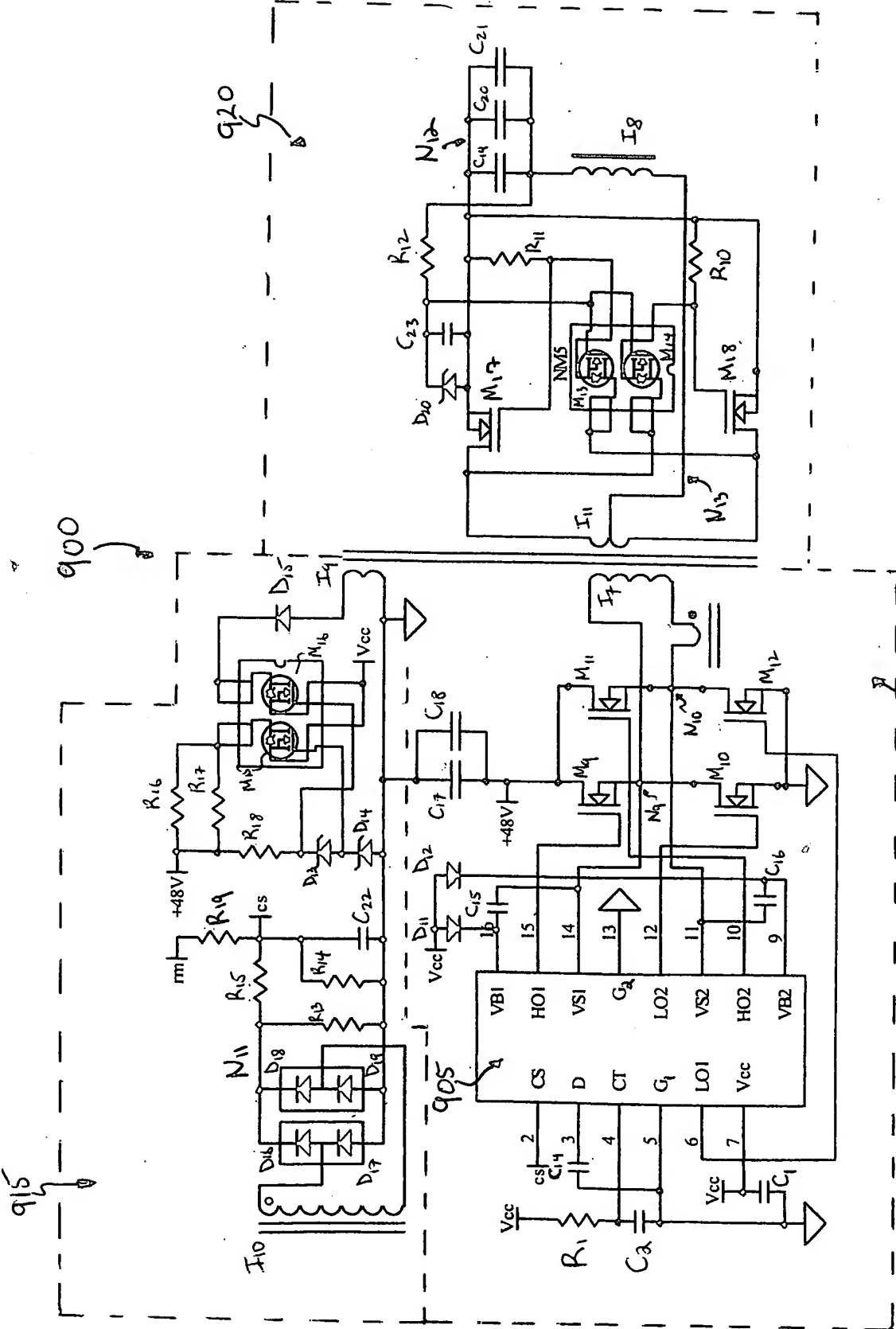
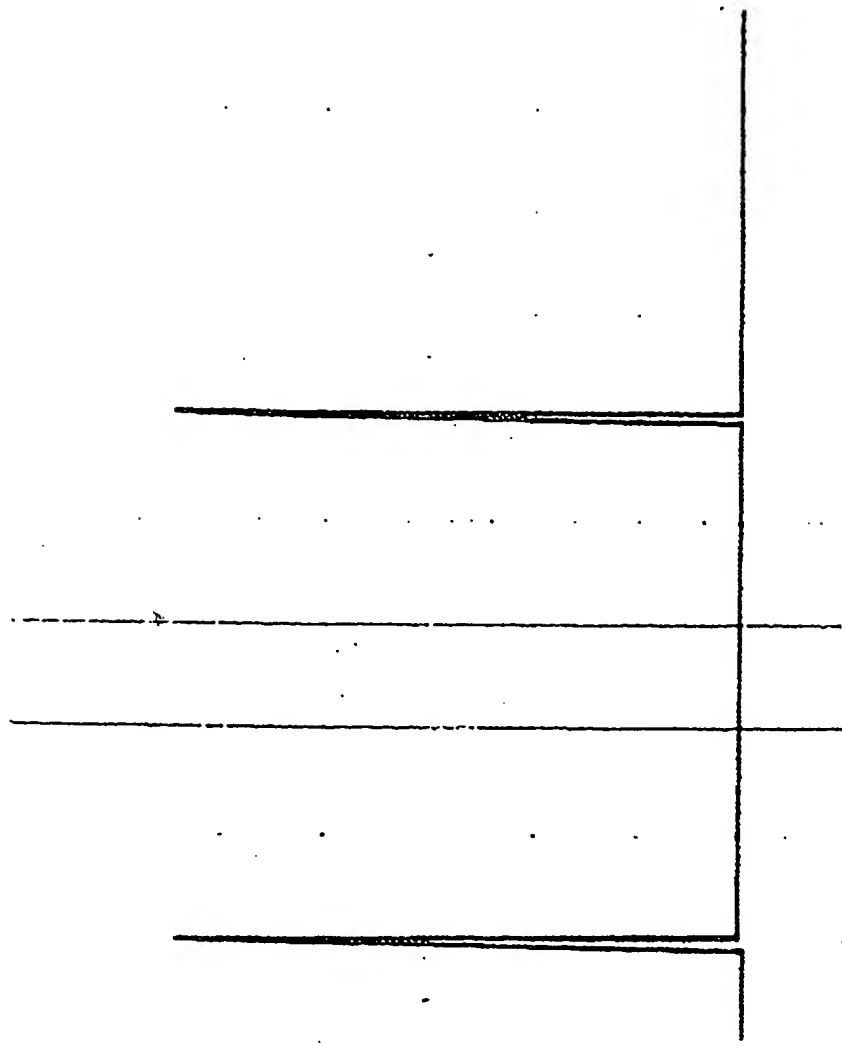


Figure 9

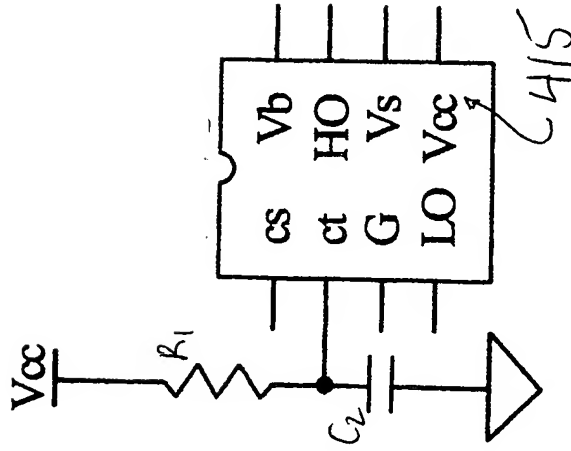




**Fig. 10: Output voltage waveform during hiccup mode at current limit setting of 21A, current load setting 22A and input voltage 48V**

Figure 11

### Self-oscillating mode



### Synchronized mode

